REMARKS

In the Office Action mailed June 14, 2005, claims 1-4, 6-27 are rejected under 35 USC §102(e) as being anticipated by Nadeau-Dostie et al., US Patent 6,829,730, (hereinafter "Nadeau-Dostie"). Claim 5 is rejected under 35 USC §103(a) as being obvious in view of Nadeau-Dostie. In response to the rejections, Applicant has amended the claims to more clearly distinguish over Nadeau-Dostie. However, in order to more clearly show how Applicant's claims distinguish over Nadeau-Dostie, Applicant will describe the circuit and operation of Nadeau-Dostie in detail before discussing the specific claim amendments for each claim.

Nadeau-Dostie is directed to a circuit having multiple test access ports (TAPS). A Master TAP functions as the circuit test bus for controlling data transfer operations with the remaining secondary TAPs in the circuit. The secondary TAPs in one or more TAP groups are connected between the circuit TDI and circuit TDO. A selection code stored in the Master TAP instruction register is loaded with each instruction. The selection code specifies the TAP group that will be involved in a data transfer operation. A TDO selector responds to the selection code by connecting the group TDO of the specified group to the circuit TDO. However, as can be seen in Figs. 2 and 3, if a TAP group other than the Master TAP group is selected, the instruction register of the Master TAP group is bypassed (or in some cases, some of the TAP elements of the instruction register of the Master TAP group are used as padding elements for other TAP groups. In particular, as shown in Fig. 2, if the Master TAP is selected, the selection code selects the TDO output of the Master TAP. That is, multiplexers 34 and 42 select the output of the shift register 30 of the Master TAP as the circuit output TDO. However, if a TAP group other than the Master TAP is selected, multiplexers 40 and 42 will bypass the Master TAP by coupling the circuit TDI to eTDI of that TAP group. The circuit TDO will then be based upon eTDO (i.e. the last TAP of the TAP group). (Col. 8, lines 19-40). Accordingly, either the Master TAP or another TAP group will be selected to generate an output.

To simplify instruction loading operations, the length of the TDI-TDO path through each TAP group is the same for all groups, including the Master TAP group.

A "padding register" may be added to make all of the instruction registers of the various TAP groups equal. (Col. 2, lines 36-63). As shown in Fig. 3, the padding register comprises the necessary number of elements of the Master TAP so that the total number of elements equals the elements of the Master TAP (including the selection elements). In order to ensure that the length of each TAP group is as long as the Master TAP, the master TAP is selected based upon the length of the longest group of embedded TAPS. That is, the number of bits of the Master TAP is equal to the combined length of the instruction registers of the longest TAP group plus the number of bits necessary to select the TAP group. (Col. 7, lines 20-50). Accordingly, when a TAP group other than the Master TAP is selected, elements of the Master TAP may be used to pad the TAP group in order to ensure that the length of the TAP group is as long as the Master TAP (i.e. the length of all of the TAP groups is the same). Accordingly, Nadeau-Dostie discloses a master tap having a fixed length based upon the length of all of the TAP groups and the number of TAP groups. However, as will be described below with respect to each independent claim, Applicant's claims as amended clearly distinguish over Nadeau-Dostie.

Independent Claim 1

Independent claim 1 is directed to a method for flexibly nesting JTAG TAP controllers for IP cores in a FPGA-based system-on-chip (SoC). In response to the rejection, Applicant has amended claim 1 to include a step of "selecting an IP core JTAG TAP controller to be coupled in series with a host JTAG TAP controller." Applicant has further amended claim 1 to indicate that the step of extending an apparent length of an instruction register of a host JTAG TAP controller comprises extending the apparent length of the instruction register "based upon the length of said instruction register of said host JTAG TAP controller and the length of an instruction register of said selected IP core JTAG TAP controller." Applicant respectfully submits that Nadeau-Dostie fails to disclose or suggest extending the apparent length of the instruction register based upon the length of the instruction register of the host JTAG TAP controller and the length of an instruction register of the selected IP core JTAG

TAP controller. Applicant submits that claim 1 as amended, and dependent claims 2-6, clearly distinguish over Nadeau-Dostie, and respectfully request reconsideration of the claims as amended.

Independent Claim 7

Independent claim 7 is directed to a method for flexibly accessing nested JTAG TAP controllers for IP cores in a FPGA-based SoC. Claim 7 as amended comprises a step of selecting an apparent register size of an instruction register of the host JTAG TAP controller based upon "the size of an instruction register for said at least one IP core JTAG TAP controller and the size of said instruction register of said host JTAG TAP controller."

In contrast to claim 7, Nadeau-Dostie selects a register size of an instruction register based upon the largest register for any TAP or group of TAPS coupled in the TDI-TDO path of Master TAP 100 and the number of TAP groups, as described above. Accordingly, Applicant submits that claim 7 as amended clearly distinguishes over Nadeau-Dostie, and that claim 7 and dependent claims 8-10 are allowable over Nadeau-Dostie.

Independent Claim 11

Claim 11 is directed to a system for flexibly accessing nested JTAG TAP controllers for IP cores in a FPGA-based SoC. The system of claim 11 comprises a selector for selecting at least one available bit of a selectable bit register to extend an apparent length of an instruction register of the host JTAG TAP controller "coupled in series with an IP core JTAG TAP controller" by using the selected at least one available bit from the selectable bit register "to accommodate a length of an instruction register of said IP core JTAG TAP controller and a length of said instruction register of said host JTAG TAP controller."

In addition to failing to disclose a host JTAG TAP controller is coupled in series with an IP core JTAG TAP controller, Nadeau-Dostie uses bits of a shift register (e.g. shift register 36) to determine which TAP group is selected. In contrast,

Applicant claims using a selected at least one available bit to accommodate a certain length of an instruction register. Further, the instruction register of the Master TAP is fixed based upon the length of the longest TAP group and the number of TAP groups to be selected. Accordingly, Applicant submits that claim 11 as amended clearly distinguishes over Nadeau-Dostie, and that claim 11 and dependent claims 12-13 are allowable over Nadeau-Dostie.

Independent Claim 14

Independent claim 14 is directed to a system for flexibly accessing nested JTAG TAP controllers for IP cores in a FPGA-based SoC. The system comprises "an instruction register size select signal enabling the selection of an apparent register size." Applicant has amended the claim to recite an instruction register size select signal enabling the selection of an apparent register size "of an instruction register of said host JTAG TAP controller based upon a size of an instruction register of said at least one IP core JTAG TAP controller and a size of said instruction register of said host JTAG TAP controller."

However, in contrast to Applicant's claims, the instruction register of the Master TAP of Nadeau-Dostie is fixed based upon the length of the longest TAP group and the number of TAP groups to be selected (as set forth above with respect to claim 11). Accordingly, Applicant submits that claim 14 as amended clearly distinguishes over Nadeau-Dostie, and that dependent claims 15-17 are allowable over Nadeau-Dostie for the same reasons that claim 14 is believed allowable. Accordingly, Applicant respectfully requests reconsideration of the claims in view of the amendment to claim 14.

Independent Claim 18

Independent claim 18 is directed to a method for ensuring an information register length for nested JTAG TAP controllers for IP cores remains the same "before and after a configuration of an FPGA" in an FPGA-based system-on-chip (SoC). The method comprises step of:

> "forming instruction registers for the IP cores that are in series with the instruction registers of the FPGA of the SoC;
>
> forming connections between FPGA JTAG logic of the FPGA and IP Core JTAG logic of the IP core using a programmable interconnect; and
>
> emulating an instruction register of the IP core prior to configuration of the FPGA using a shift register of the same length as the instruction register of the IP core."

Applicant respectfully submits that Nadeau-Dostie fails to disclose or suggest any of the steps of claim 18. There is no mention in the Office Action of the disclosure of an FPGA as claimed by Applicant. More specifically, Nadeau-Dostie fails to disclose or suggest (i) forming connections between FPGA JTAG logic of the FPGA and IP Core JTAG logic of the IP core using a programmable interconnect, or (ii) emulating an instruction register of the IP core prior to configuration of the FPGA. Accordingly, Applicant respectfully submits that independent claim 18 and dependent claims 19-20 are allowable over Nadeau-Dostie, and respectfully requests reconsideration of the claims.

Independent Claim 21

Independent claim 21 is directed to a system for performing boundary scan functions on a plurality of IP cores. The system of claim 21 comprises a host JTAG TAP controller coupled to each of the first JTAG TAP controllers, the host JTAG TAP controller comprising a selectable bit register "enabling the selection of an apparent register size of an instruction register of the host JTAG TAP controller based upon a size of an instruction register of the first JTAG TAP controller for each IP core of the plurality of IP cores and the size of the instruction register of the host JTAG TAP controller."

Applicant submits that Nadeau-Dostie fails to disclose or suggest a host JTAG TAP controller comprising a selectable bit register enabling the selection of an apparent register size of an instruction register of the host JTAG TAP controller "based upon a size of an instruction register of the first JTAG TAP controller for each

IP core of the plurality of IP cores and the size of the instruction register of the host JTAG TAP controller" as set forth in claim 21 as amended. Accordingly, Applicant respectfully submits that claim 21 and dependent claims 22-27 are allowable over Nadeau-Dostie, and respectfully requests reconsideration of the claims.

CONCLUSION

All claims are in condition for allowance and a Notice of Allowance is respectfully requested. If there are any questions, the Applicant's attorney can be reached at Tel: 408-879-6149 (Pacific Standard Time).

Respectfully submitted,

Kim Kanzaki, Ph.D.
Attorney for Applicant
Reg. No. 37,652

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on August 15, 2005.

Pat Slaback — Pat Slaback
Name *Signature*